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PATENT APPLICATION

ATTORNEY DOCKET NO. 200315654-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Manish K. Ahluwalia

Confirmation No.: 1055

Application No.: 10/790,509

Examiner: Zhuo H. Li

Filing Date: March 1, 2004

Group Art Unit: 2185

Title: MEMORY MANAGEMENT

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on June 25, 2008.

☒ The fee for filing this Appeal Brief is $510.00 (37 CFR 41.20).

☐ No Additional Fee Required.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120	☐ 2nd Month $460	☐ 3rd Month $1050	☐ 4th Month $1640

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 510. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees.

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Date of facsimile: 07/30/2008
Typed Name: Jennifer L. Vomhof
Signature:

Respectfully submitted,
Manish K. Ahluwalia
By

Edward J. Brooks III
Attorney/Agent for Applicant(s)
Reg No.: 40,925
Date: 07/30/2008
Telephone: (612) 236-0120

Rev 10/07(ApiBrief)

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Respectfully submitted,
Manish K. Ahluwalia
By

Edward J. Brooks III
Attorney/Agent for Applicant(s)
Reg No.: 40,925
Date: 07/30/2008
Telephone: (612) 236-0120

Rev 10/07(AplBrief)

Docket No.: 200315654-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	10/790,509
Appellants:	:	Manish Ahluwalia
Filed:	:	March 1, 2004
TC/A.U.	:	2185
Examiner:	:	Zhuo H. Li
Title	:	MEMORY MANAGEMENT

APPEAL BRIEF

MS APPEAL BRIEF-PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir or Madame:

This brief, in compliance with 37 C.F.R. § 41.37, is in furtherance of the Notice of Appeal filed under 37 C.F.R. § 41.31 on June 25, 2008.

This brief is accompanied by the fee set forth in 37 CFR § 41.20(b)(2), as described in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37:

I. Real Party In Interest

II. Related Appeals and Interferences

III. Status of Claims

IV. Status of Amendments

V. Summary of Claimed Subject Matter

VI. Grounds of Rejection to be Reviewed on Appeal

VII. Argument

VIII. Claims Appendix

IX. Evidence Appendix

X. Related Proceedings Appendix

The final page of this brief bears the attorney's signature.

I. REAL PARTY IN INTEREST

The real parties in interest for this appeal are:

A. The Hewlett-Packard Development Company, LP, a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"); and

B. HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

II. RELATED APPEALS AND INTERFERANCES

Appellant submits that no related application is presently undergoing appeal or interference proceedings.

III. STATUS OF CLAIMS

A. Total Claims: 1-23

B. Current Status of Claims:

1. Claims canceled: none
2. Claims withdrawn: none
3. Claims pending: 1-23
4. Claims allowed: none
5. Claims rejected: 1-23
6. Claims objected to: none

C. Claims on Appeal: 1-23

IV. STATUS OF AMENDMENTS

Appellant has not filed any amendments to the application subsequent to the Final Office Action dated June 19, 2008.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A. Independent claim 1

Independent claim 1 recites a computing device that includes a processor (Page 5, line 22, through page 6, line 5; and Figure 1), and a memory coupled to the processor (Page 5, lines 22-29; page 6, lines 6-20; and Figure 1). The computing device also includes program instructions provided to the memory and executable by the processor to track a virtual address space for a process associated with a device connected to the computing device (Page 8, lines 3-18; page 8, line 31, through page 9, line 23; page 11, line 18, through page 12, line 3; page 12, line 29, through page 13, line 6; page 13, line 17, through page 14, line 28; page 16, lines 1-6; page 16, lines 22-27; page 19, lines 24-32; page 21, line 3, through page 23, line 15; and Figures 2A-2B, 3A, and 5), release a physical address space associated with the virtual address space when the device has a connection removed from the computing device (Page 4, lines 24-31; page 8, lines 3-30; page 11, line 18, through page 13, line 6; page 13, line 17, through page 14, line 28; page 16, lines 7-9; page 16, lines 27-30; page 17, lines 1-8; page 18, lines 6-13; page 19, lines 6-23; page 20, lines 1-16; page 21, lines 3-18; page 22, lines 30-33; page 23, line 10, through page 24, line 8; and Figures 2A, and 4-5), register by providing an indication in the virtual memory data structure for the process that the virtual address space, previously available to the process, is no longer valid for process use (Page 4, line

31, through page 5, line 2; page 6, lines 15-20; page 10, line 9, through page 15, line 32; page 16, lines 9-17; page 16, lines 30-32; page 17, lines 4-14; page 18, line 13, through page 19, line 23; page 20, lines 19-26; page 23, lines 16-28; page 24, line 24, through page 25, line 2; and Figures 1, 2C, 3A-3B, and 4-5), wherein registering is triggered by detection that the physical address space that was being used by processes associated with the device has been released (Page 20, line 30, through page 21, line 2; and page 23, lines 16-28), and wherein the registering occurs as the physical address space is released and before release of the virtual address space by the process (Page 4, line 24, through page 5, line 2; page 20, line 17, through page 21, line 2; page 23, lines 16-28; and Figure 5).

Independent claim 1 is argued together with dependent claims 2 and 6. Dependent claims 3-5 and 7 are argued separately from independent claim 1.

1. Claim 2 depends from independent claim 1 and recites that the device includes a device which can be mapped to memory (Page 6, lines 21-33; page 8, lines 1-30; page 16, lines 1-6; page 16, lines 22-27; page 18, lines 1-12; page 19, line 6, through page 20, line 4; page 21, lines 3-18; page 24, line 31, through page 25, line 2; and Figures 2A and 4-5).

2. Claim 3 depends from independent claim 1 and recites that the virtual address space includes an input/output space (Page 16, lines 7-12).

3. Claim 4 depends from independent claim 1 and recites that the program instructions are part of a memory management system which includes a virtual memory data structure associated with the process (Page 6, lines 8-20; page 10, line 9, through page 15, line 32; page 16, lines 7-32; page 17, lines 4-14; page

18, line 1, through page 19, line 32; page 22, line 13, through page 25, line 2; and Figures 1, 2C, 3A-3B, and 4).

4. Claim 5 depends from dependent claim 4 and recites that the program instructions execute to register the virtual address space is no longer valid for process use in the virtual memory data structure associated with the process (Page 4, line 24, through page 5, line 2; page 16, line 7, through page 17, line 19; page 18, lines 13-20; page 19, lines 6-23; and page 24, line 24, through page 25, line 2).

5. Claim 6 depends from independent claim 1 and recites that the program instructions execute to allocate the virtual address space when the process requests physical memory (Page 11, line 18, through page 12, line 3; page 12, line 21, through page 13, line 7; page 14, lines 11-28; page 16, lines 18-20; page 19, lines 6-23; page 20, line 1, through page 21, line 2; page 22, line 13, through page 23, line 9; and page 23, line 29, through page 24, line 23).

6. Claim 7 depends from independent claim 1 and recites that the program instructions execute to register that the virtual address space is available for use when the process releases the virtual address space (Page 16, lines 18-22; and page 23, lines 16-20).

B. Independent claim 8

Independent claim 8 recites a computing device that includes a processor (Page 5, line 22, through page 6, line 5; and Figure 1), and a random access memory coupled to the processor (Page 5, lines 22-29; page 6, lines 6-20; and Figure 1). The computing device also includes program instructions provided to the memory and

executable by the processor, the program instructions are part of a memory management system to dereference a virtual address space for a process associated with a removable memory mappable device connected to the computing device (Page 5, lines 22-29; page 6, lines 8-33; page 8, line 1, through page 9, line 23; page 11, line 10, through page 12, line 3; page 13, line 17, through page 14, line 28; page 16, lines 1-32; page 18, lines 1-12; page 19, line 6, through page 20, line 4; page 21, line 3, through page 22, line 12; page 22, line 13, through page 25, line 2; and Figures 1, 2A-2B, 3A, and 4-5), release a physical address space associated with the virtual address space when the device associated with the process is logically disconnected (Page 4, lines 24-31; page 8, lines 3-30; page 11, line 18, through page 13, line 6; page 13, line 17, through page 14, line 28; page 16, lines 27-30; page 17, lines 1-8; page 18, lines 6-13; page 19, lines 6-23; page 20, lines 1-16; page 21, lines 3-18; page 22, lines 30-33; page 23, line 10, through page 24, line 8; and Figures 2A, and 4-5), and register by providing an indication in the virtual memory data structure for the process that the virtual address space is no longer available to the process (Page 4, line 31, through page 5, line 2; page 6, lines 15-20; page 10, line 9, through page 15, line 32; page 16, lines 9-17; page 16, lines 30-32; page 17, lines 4-14; page 18, line 13, through page 19, line 23; page 20, lines 19-26; page 23, lines 16-28; page 24, line 24, through page 25, line 2; and Figures 1, 2C, 3A-3B, and 4-5), wherein to register is triggered by detection that the physical address space that was being used by processes associated with the device has been released (Page 20, line 30, through page 21, line 2; and page 23, lines 16-28), and wherein to register occurs as the physical address space is released and before release of the

virtual address space by the process (Page 4, line 24, through page 5, line 2; page 20, line 17, through page 21, line 2; page 23, lines 16-28; and Figure 5).

Independent claim 8 is argued together with dependent claim 10. Dependent claims 9 and 11-12 are argued separately from independent claim 8.

1. Claim 9 depends from independent claim 8 and recites that the program instructions execute to unmap the virtual address space in a manner which do not violate semantics for an operating system of the computing device (Page 5, lines 3-15; page 17, lines 1-19; page 19, lines 6-23; page 20, lines 17-24; page 24, lines 9-14; and Figure 5).

2. Claim 10 depends from dependent claim 9 and recites that the operating system is selected from the group of a Unix operating system and a Linux operating system (Page 5, lines 3-15; page 7, line 32, through page 8, line 2; page 9, lines 24-27; and page 17, lines 1-4).

3. Claim 11 depends from independent claim 8 and recites that the program instructions execute to allow the process to unmap the virtual address space subsequent to the release of the physical address space (Page 4, line 27, through page 5, line 7; and page 17, lines 1-19).

4. Claim 12 depends from independent claim 8 and recites that the program instructions execute to indicate an operation as failed if the process attempts to perform the operation subsequent to registering that the virtual address space is no longer valid for process use (Page 5, lines 3-10; page 17, lines 1-17; and page 19, lines 6-20).

C. Independent claim 13

Independent claim 13 recites a processor (Page 5, line 22, through page 6, line 5; and Figure 1) and a memory coupled to the processor (Page 5, lines 22-29; page 6, lines 6-20; and Figure 1), the memory including program instructions for maintaining a virtual memory data structure as part of a memory management system (Page 6, lines 8-20; page 10, line 9, through page 15, line 32; page 16, lines 7-32; page 17, lines 4-14; page 18, line 1, through page 19, line 32; page 22, line 13, through page 25, line 2; and Figures 1, 2C, 3A-3B, and 4). The computing device also includes means for unmapping a virtual address space for a process that is triggered as a physical address space used by the process is being released, in a manner which does not violate semantics for an operating system of the computing device, when a removable memory mappable device associated with the process is logically disconnected (Page 4, line 24, through page 5, line 15; page 5, lines 22-29; page 6, lines 21-33; page 8, lines 1-30; page 8, line 31, through page 9, line 23; page 11, line 18, through page 13, line 6; page 13, line 17, through page 14, line 28; page 16, lines 1-9; page 16, lines 22-30; page 17, lines 1-19; page 18, lines 1-13; page 19, line 6, through page 20, line 24; page 20, line 30, through page 21, line 18; page 22, line 13, through page 24, line 14; page 24, line 24, through page 25, line 2; and Figures 2A-2B, 3A, and 4-5).

Independent claim 13 is argued together with dependent claims 14-15 and 17. Dependent claims 16 and 18 are argued separately from independent claim 13.

1. Claim 14 depends from independent claim 13 and recites that the program instructions execute to dereference the virtual address space for the

process (Page 11, lines 25-28; page 16, lines 22-27; page 18, lines 1-6; page 19, lines 24-32; and Figures 4-5).

2. Claim 15 depends from independent claim 13 and recites that the means for unmapping the virtual address space includes program instructions which execute to maintain a representation of an object associated with the process in the virtual memory data structure of the process (Page 11, lines 29-31; page 17, lines 1-7; page 18, line 1, through page 19, line 23; page 20, lines 27-30; page 24, lines 24-28; and Figure 4).

3. Claim 16 depends from dependent claim 15 and recites that the means for unmapping the virtual address space includes program instructions which execute to remove a mapping of the object to physical memory (Page 17, lines 7-8; page 18, lines 10-12; and Figure 4).

4. Claim 17 depends from dependent claim 16 and recites that the means for unmapping the virtual address space includes program instructions which execute to register in the virtual memory data structure of the process that the virtual address space associated with the process is not available for use subsequent to when the mapping of the object to physical memory has been removed (Page 4, line 24, through page 5, line 7; page 16, lines 7-17; page 16, line 30, through page 17, line 19; and page 24, lines 28-31).

5. Claim 18 depends from dependent claim 17 and recites that the program instructions execute to set a bit in a pregion of the virtual memory data structure to indicate that the virtual address space is not available for use (Page 13,

line 17, through page 14, line 28; page 17, lines 1-14; page 18, line 1, through page 19, line 5; and Figures 3A and 4).

D. Independent claim 19

Independent claim 19 recites a method for memory management on a computing device that includes dereferencing a memory address for a process associated with a removable memory mappable device (Page 5, lines 22-29; page 6, lines 21-33; page 8, lines 1-30; page 11, lines 25-28; page 16, lines 1-6; page 16, lines 22-27; page 17, lines 1-6; page 18, lines 1-12; page 19, line 6, through page 20, line 4; page 21, line 2, through page 22, line 12; page 23, lines 16-28; page 24, line 9, through page 25, line 2; and Figures 1, 2A, and 4-5), mapping a representation of an object associated with the process in a virtual memory data structure associated with the process (Page 4, line 31, through page 5, line 2; page 6, lines 8-33; page 8, lines 3-30; page 10, line 9, through page 15, line 32; page 16, lines 1-32; page 17, lines 1-14; page 18, line 1, through page 19, line 23; page 20, lines 1-3; page 20, line 28, through page 21, line 19; page 24, line 24, through page 25, line 2; and Figures 1, 2A, 2C, 3A-3B, and 4), removing the object from physical memory when the device is logically disconnected from the computing device (Page 4, lines 24-31; page 8, lines 3-30; page 11, line 18, through page 13, line 6; page 13, line 17, through page 14, line 28; page 16, lines 7-9; page 16, lines 27-30; page 17, lines 1-8; page 18, lines 6-13; page 19, lines 6-23; page 20, lines 1-16; page 21, lines 3-18; page 22, lines 30-33; page 23, line 10, through page 24, line 8; and Figures 2A, and 4-5), and providing an indication in the virtual memory data structure for the process that a virtual address space is no longer available for use by

the process as triggered by detection of a physical address space used by the process being released and when the object is removed from physical memory, without removing the representation of the object from the virtual memory data structure for the process (Page 4, line 31, through page 5, line 2; page 6, lines 15-20; page 10, line 9, through page 15, line 32; page 16, lines 9-17; page 16, lines 30-32; page 17, lines 1-14; page 18, line 1, through page 19, line 23; page 20, line 19, through page 21, line 2; page 23, lines 16-28; page 24, line 24, through page 25, line 2; and Figures 1, 2C, 3A-3B, and 4-5).

Independent claim 19 is argued separately from dependent claims 20-21.

1. Claim 20 depends from independent claim 19 and recites that the method further includes unmapping the virtual address space at the request of the process subsequent to the device being logically disconnected from the computing device (Page 4, line 27, through page 5, line 7; and page 17, lines 1-19).

2. Claim 21 depends from independent claim 19 and recites that the method further includes indicating an operation as failed if the process attempts to perform the operation subsequent the device being logically disconnected from the computing device (Page 5, lines 3-10; page 17, lines 1-17; and page 19, lines 6-20).

E. Independent claim 22

Independent claim 22 recites a method for memory management that includes tracking a virtual address space for a process associated with a removable memory mappable device connected to a computing device (Page 6, lines 21-33; page 8, line 3, through page 9, line 23; page 11, line 18, through page 12, line 3;

page 12, line 29, through page 13, line 6; page 13, line 17, through page 14, line 28; page 16, lines 1-6; page 16, lines 22-27; page 18, lines 1-12; page 19, line 6, through page 20, line 4; page 21, line 3, through page 23, line 15; page 24, line 31, through page 25, line 2; and Figures 2A-2B, 3A, 4 and 5), releasing a physical address space when the device has a logical connection removed from the computing device (Page 4, lines 24-31; page 8, lines 3-30; page 11, line 18, through page 13, line 6; page 13, line 17, through page 14, line 28; page 16, lines 7-9; page 16, lines 27-30; page 17, lines 1-8; page 18, lines 6-13; page 19, lines 6-23; page 20, lines 1-16; page 21, lines 3-18; page 22, lines 30-33; page 23, line 10, through page 24, line 8; and Figures 2A, and 4-5), and at the release of the physical address space used by the process and before the process has released the virtual address space, registering an indication in a virtual memory data structure for the process that the virtual address space is not available to the process in a manner which does not violate semantics of an operating system (Page 4, line 24, through page 5, line 15; page 6, lines 8-20; page 10, line 9, through page 15, line 32; page 16, lines 7-32; page 17, lines 1-19; page 18, line 1, through page 19, line 23; page 20, line 17, through page 21, line 2; page 23, lines 16-28; page 24, lines 9-14; page 24, line 24, through page 25, line 2; and Figures 1, 2C, 3A-3B, and 4-5).

F. Independent claim 23

Independent claim 23 recites a computer readable medium having computer readable instructions stored thereon for execution by a device to perform a method (Page 7, lines 8-17). The method includes dereferencing a virtual address space for a process associated with a removable memory mappable device as part of a

memory management system on a computing device (Page 5, lines 22-29; page 6, lines 8-33; page 8, line 1, through page 9, line 23; page 11, line 10, through page 12, line 3; page 13, line 17, through page 14, line 28; page 16, lines 1-32; page 18, lines 1-12; page 19, line 6, through page 20, line 4; page 21, line 3, through page 22, line 12; page 22, line 13, through page 25, line 2; and Figures 1, 2A-2B, 3A, and 4-5), releasing a physical address space when the device is logically disconnected from the computing device (Page 4, lines 24-31; page 8, lines 3-30; page 11, line 18, through page 13, line 6; page 13, line 17, through page 14, line 28; page 16, lines 7-9; page 16, lines 27-30; page 17, lines 1-8; page 18, lines 6-13; page 19, lines 6-23; page 20, lines 1-16; page 21, lines 3-18; page 22, lines 30-33; page 23, line 10, through page 24, line 8; and Figures 2A, and 4-5), and at the release of the physical address space used by the process and before the process has released the virtual address space, registering an indication in a virtual memory data structure for the process that the virtual address space is no longer available to the process in a manner which does not violate semantics for an operating system the computing device (Page 4, line 24, through page 5, line 15; page 6, lines 8-20; page 10, line 9, through page 15, line 32; page 16, lines 7-32; page 17, lines 1-19; page 18, line 1, through page 19, line 23; page 20, line 17, through page 21, line 2; page 23, lines 16-28; page 24, lines 9-14; page 24, line 24, through page 25, line 2; and Figures 1, 2C, 3A-3B, and 4-5).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether or not independent claim 23 is unpatentable under 35 USC § 101 because the claim is allegedly directed to non-statutory subject matter.